

**Serial No.: 10/700,557**

### REMARKS

This Amendment is being filed in response to the Office Action dated October 5, 2004. For the following reasons, this application should be considered in condition for allowance and the case passed to issue.

Claims 1-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lo et al., U.S. Patent No. 6,791,155 (hereafter "Lo"). This rejection is hereby traversed and reconsideration and withdrawal thereof are respectfully requested. The following is a comparison of the present invention with the Lo reference.

The present invention, as currently claimed, relates to a method of forming a semiconductor device comprising the steps of providing a substrate and forming a trench in the substrate, this trench including opposite sidewalls extending upwardly from a base of the trench. At least two insulating layers are deposited into the trench to form a shallow trench isolation structure. An innermost one of the insulating layers substantially conforms to the base and the two sidewalls of the trench. An outermost of the insulating layers spans the sidewalls of the trench so that a gap is formed between the insulating layers in the trench.

The gap formed between the insulating layers in the trench creates compressive forces within the shallow trench isolation structure. This, in turn, creates tensile stress within the surrounding substrate to thereby enhance mobility of the semiconductor device. The Lo reference fails to show or suggest these features.

In order to anticipate claims of an invention under 35 U.S.C. § 102, a single prior art reference must identically disclose each and every element of the claimed invention. However, Lo fails to identically disclose each of the elements of the claimed invention. As shown in Lo, a first dielectric layer 130 is formed within a trench 105 in a semiconductor substrate 100. A

**Serial No.: 10/700,557**

second dielectric layer 140 is deposited within the first dielectric layer. A gap 145 is created entirely within the second dielectric layer 140. This gap is said to substantially reduce the stress between the trench dielectric layer and the surrounding semiconductor substrate, providing a method of minimizing or reducing mechanical stress in current standard STI process.

In contrast to the claimed invention, gap 145 is entirely within the single, second dielectric layer 140. The gap is not provided between the insulating layers in the trench, as required by claim 1 of the present invention. Lo, therefore, cannot be said to identically disclose each and every element of the claimed invention. Further, Lo seeks to minimize stress in current standard STI processes, and allow the trench dielectric layer to be expanded or shrunk with the surrounding substrate without generating stress. However, the present invention actually seeks to create tensile stress within the surrounding substrate and accomplishes this by creating compressive forces within the shallow trench isolation structure by providing insulating layers with the gap formed therebetween.

Since Lo neither shows or suggests the invention as now claimed, the rejections of the claims under 35 U.S.C. § 102(e) should be reconsidered and withdrawn. Such action is courteously solicited.

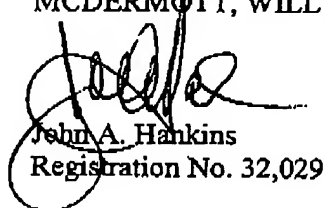
In light of the Amendments and Remarks above, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

**Serial No.: 10/700,557**

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY



John A. Hankins  
Registration No. 32,029

600 13th Street, N.W.  
Washington, DC 20005-3096  
(202) 756-8000 JAH:cej  
Facsimile: (202) 756-8087  
**Date: January 5, 2005**

**Please recognize our Customer No. 20277  
as our correspondence address.**